A 0.35µm CMOS Linear Voltage Regulator with High Voltage Power Supply

Ivelina Iliyanova Atanasova and Atanas Stoyanov Pangev

Abstract – **A CMOS linear voltage regulator with high voltage power supply is presented in this paper. The proposed regulator consists of an analog error amplifier, current sources, start-up circuit, protection circuit, feedback circuit and NMOS High Voltage (NHV) pass element. The regulator is designed for input voltages between 7V and 27V. The output voltage is 3,1V±0,2V. The simulation results show that the proposed linear voltage regulator has an excellent performance. It will be used as a part of the more complex application specific integrated circuit.**

Keywords –**Linear voltage regulator, High voltage CMOS**

I. Introduction

The linear voltage regulators are appropriate for use in different kind of automotive, portable, industrial, or medical applications [1]. The automotive industry requires low dropout regulators to power up digital circuit, especially during cold-crank conditions where the battery voltage can be below 6 V. The increasing demands are especially apparent in mobile battery-operated products, such as cellular phones, pagers, camera, recorders, and laptops [2]. As results, different kind of customer-driven solutions, appropriate for specific areas of application, are implemented [3], [4], as well new solutions are necessary to be developed [5], [6].

The paper presents the results from design and simulation of 0,35µm CMOS linear voltage regulator with high voltage power supply.

II. Circuit Description

Linear voltage regulators are designed to automatically maintain a constant output voltage level. The main components are a power MOSFET and a differential amplifier (error amplifier) (Fig. 1) [7]. One input of the differential amplifier monitors a percentage of the output, as determined by the resistor ratio of R1 and R2.

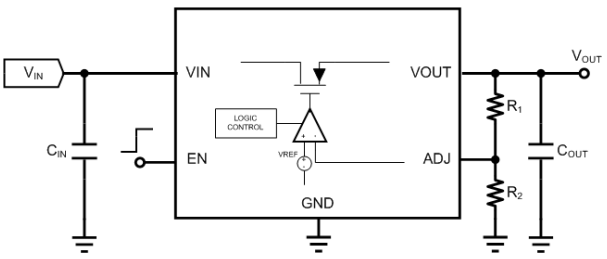

Fig. 1. Block diagram of typical linear voltage regulator

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The second input of the differential amplifier is from a stable voltage reference (band-gap reference). If the output voltage rises too high relative to the reference voltage, the drive to the power MOSFET changes so as to maintain a constant output voltage.

The block diagram of the proposed linear voltage regulator is shown on Fig. 2. It consists of an analog error amplifier (EA), current source, start-up circuit, protection circuit, feedback R1-R2 and pass element M1. The circuit is designed for input voltages between 7V and 27V. The output voltage is 3,1V±0,2V.

Fig. 3 shows the circuit topology of the proposed regulator.

A. Error Amplifier (EA)

The error amplifier has a two-stage configuration (Fig. 3). The first stage is a differential amplifier (M1-M4) and the second stage is a cascode common source – common gate configuration (M6, M8). The power supply of the first stage is the input high voltage power supply. The power supply of the second stage is the output of the regulator. This solution guarantees the stable star-up of the circuit.

Because of the transistors are low voltage and the second stage is cascode the amplifier has very good voltage gain.

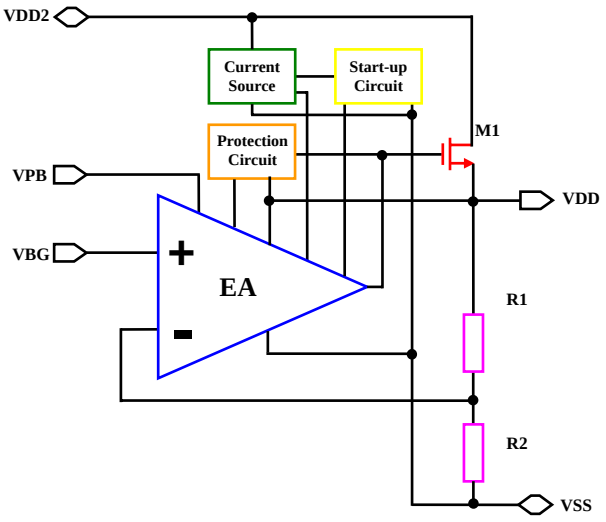

Fig. 2. Block diagram of proposed linear voltage regulator

B. Pass Transistor

The pass element M1 (Fig. 2) is a NMOST. The high value of the power supply voltage (up to 27V) imposes the using of High Voltage (NHV) transistor.

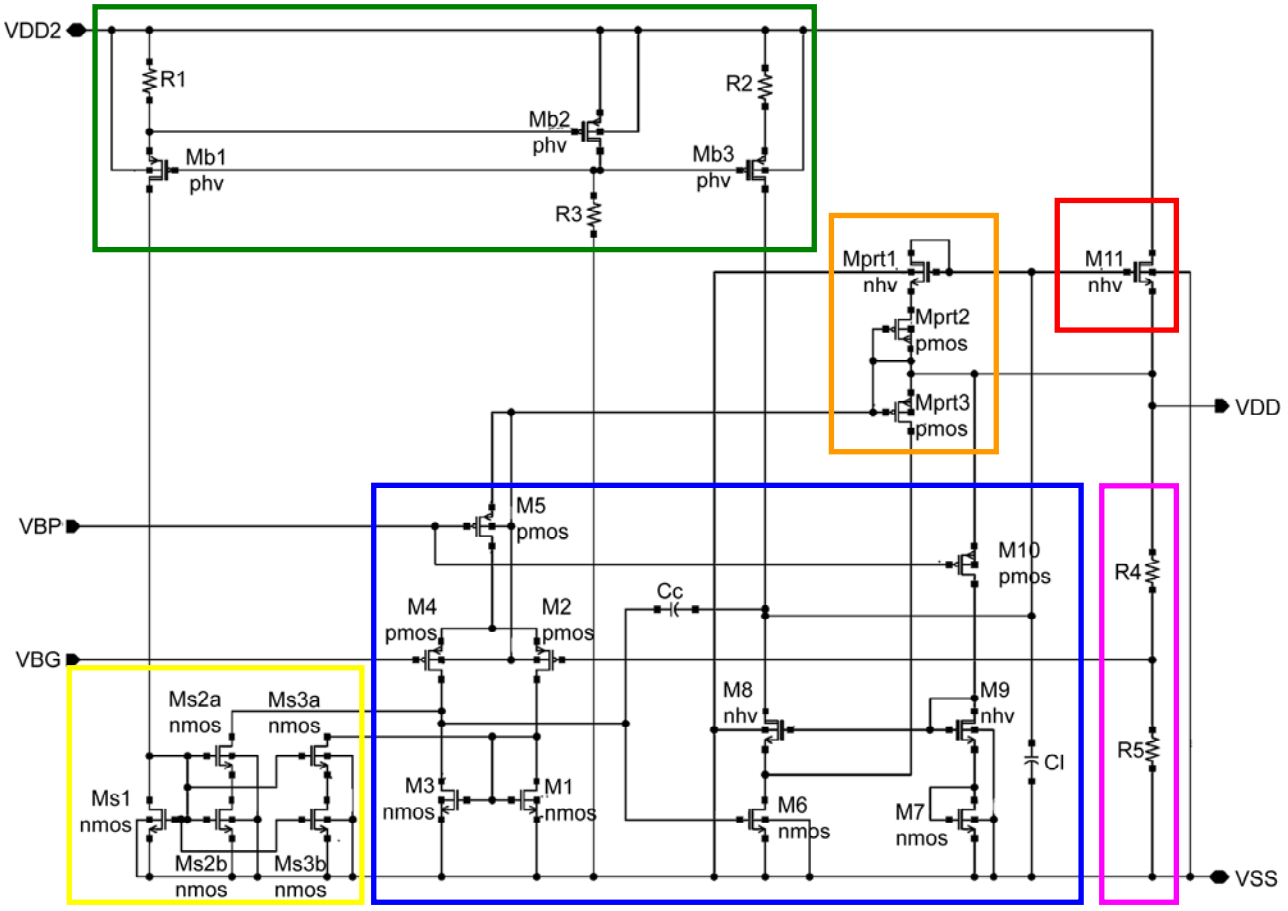

Fig. 3. Circuit topology of the regulator

The using of N-channel transistor is better then using a P-channel transistor. When the pass element is implemented by P-channel transistor, the circuit configuration is common source. The common source is a voltage gain stage and usually it is necessary frequency compensation to be applied. Another reason to choose N-channel transistor is because the power supply rejection ratio (PSRR) in the common drain configuration is better then in the common source connection.

C. Feedback

The feedback is calculated using Eq. 1.

$$\frac{V_{VDD}}{V_{VBG}} = \frac{R_4 + R_5}{R_5} \quad (1)$$

D. Band-gap Reference Circuit

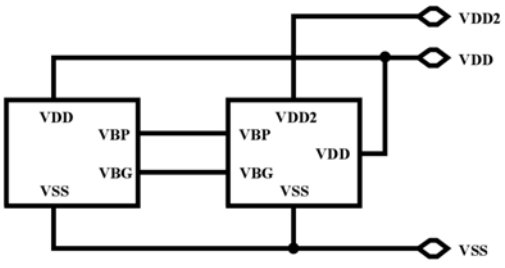

Fig. 4. Block diagram of the band-gap and the regulator circuits

The regulator is connected with band-gap source (see Fig. 4). The VBP and VBG outputs of the band-gap are inputs of the regulator (see Fig. 3). The power supply of the band-gap is coming from the regulator's output VDD.

E. Start-up Circuit

In the beginning, when the powering of the regulator is starting, the pass transistor M11 (Fig. 3) is cut-off and the voltage value at the output is low. The start-up circuit is intended to ensure the reliable setting of the different stages in operating mode in order to ensure the work of the regulating element M11 in saturation. The circuit is implemented by transistors Ms1-Ms2a-Ms2b-Ms3a-Ms3b.

F. Protection Circuit

There is a danger of high voltages in some of the regulator nodes. Therefore a protection circuit (Fig. 5) is designed. In this circuit the voltage is limited by the diode connected transistors.

Fig. 5a shows the protection circuit with CMOS transistors and Fig. 5b shows the equivalent of the same circuits using diodes only. The terminal 1 is connected to the current source; terminal 2 – to the ground; terminal 3 – to the source of M5; terminal 4 – to the gate of pass transistor; terminal 5 – to the power supply and terminal 6 – to the drain of M6.

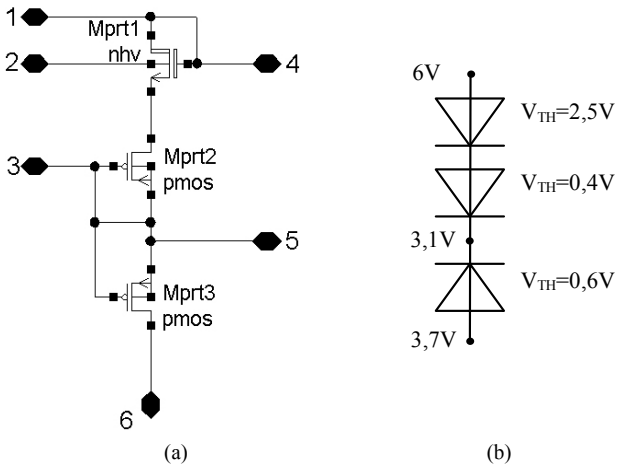

Fig. 5. Protection circuit

The part of the circuit (Mprt1- Mprt2) protects the gate of the pass element and another part (Mprt3) protects the low voltage transistor M6. So it is ensured the voltage in the gate of the pass transistor to be less than 6V and in the drain of M6 to be less than 3,7V.

G. Current Source

The current source circuits Mb1-Mb2-Mb3 ensure the stability of operation. Transistors are PHV because the power supply voltage is high.

III. Simulation Results

A. Simulation of Error Amplifier

Fig. 6 shows the amplitude-frequency and the phase-frequency characteristics of the error amplifier. The results are generalized in Table 1. As we can see the phase margin is higher than 45° and the amplifier is characterized with good stability.

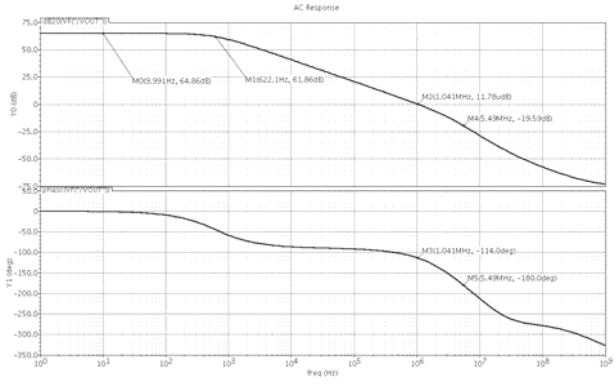

Fig. 6. The frequency response of the error amplifier

Table 1. Amplifier Parameters

Gain voltage	65dB
Gain bandwidth	622Hz
Bandwidth	1,04MHz
Gain margin	19,6dB
Phase margin	66°

B. Simulation of Output-to-input Voltage Ratio

Fig. 7 demonstrates that for the range of the input voltage between 7V and 27V, the designed linear regulator maintains output voltage of 3,1V. This satisfies the requirements of the customer.

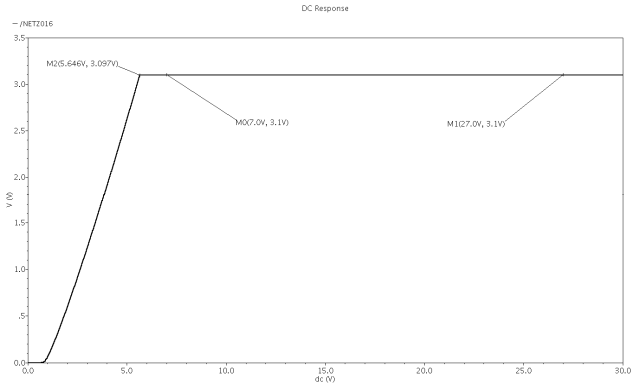

Fig. 7. Output-to-input voltage ratio

C. Simulation of Line Regulation

The line regulation is the capability of the circuit to maintain a constant output voltage level despite of the changes to the input voltage level. The line regulation is expressed as percent of change in the output voltage relative to the change in the input line voltage.

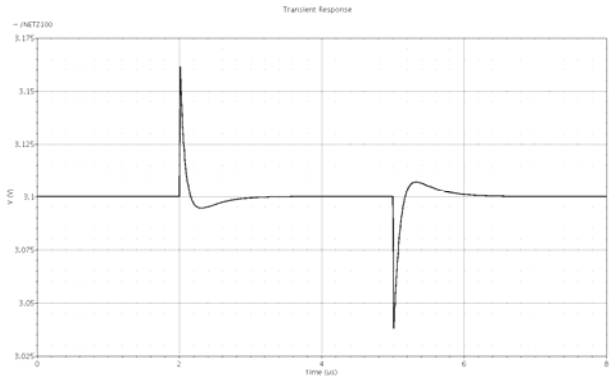

Fig. 8. Line regulation of the circuit

Fig. 8 shows the line regulation of the designed circuit. A sharp increasing and then normalization of the output voltage can be seen-on when a positive front of the input voltage signal is applied. An abrupt voltage fall, also followed by normalization of the output voltage can be seen, when there is a negative front of the input voltage signal. Output voltage remains within the limits and the attenuation is good. The coefficient of line regulation can be calculated using Eq. 2.

$$VR_{LINE} = \frac{\Delta VDD}{VDD}.100 = \frac{62.10^{-3}}{3{,}1}.100 = 2\%/V \qquad (2)$$

The obtained result (2%/V) satisfies the customer's specifications.

D. Simulation of Load Regulation

The load regulation is the capability to maintain a constant voltage (or current) level at the output despite of the changes in the load.

In Fig. 9 is shown that when there is a positive front of the output current signal, the output voltage abruptly decreases and after that gradually comes back to normal. When there is a negative front of the output current signal, it can be seen the same, but here the voltage is rising abruptly and then coming back to normal. The rising and the decreasing of the voltage are in the normal limits. The attenuation is perfect. The coefficient of load regulation is calculated using Eq. 3.

$$VR_{LOAD} = \frac{\Delta VDD}{VDD}.100 = \frac{37.10^{-3}}{3{,}1}.100 = 1{,}2\% / mA \qquad (3)$$

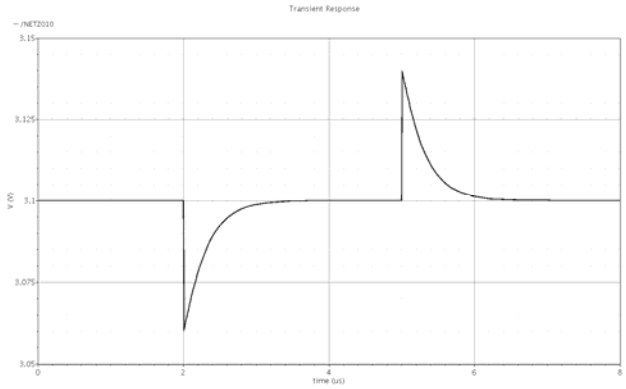

Fig. 9. Load regulation

E. Simulation of Power Supply Rejection Ratio (PSRR)

The PSRR is defined as the ratio of the change in supply voltage to the corresponding change in output voltage of the device. The simulation result (Fig. 10) shows that PSRR is 30,53dB with bandwidth 1,041MHz.

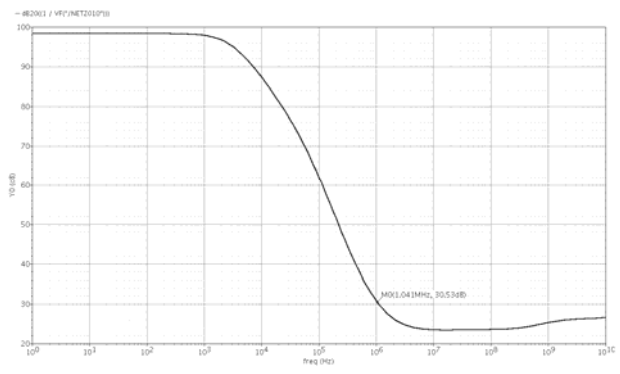

Fig. 10. PSRR of proposed regulator

F. Simulation of Temperature Drift of Output Voltage

The temperature drift of output voltage is the dependence of the output voltage on the temperature.

Fig. 11 shows a very low temperature dependency of the output voltage. In the temperature range from -40°C to 150°C the change of the output voltage is about 250µV. This corresponds entirely to the customer's specifications.

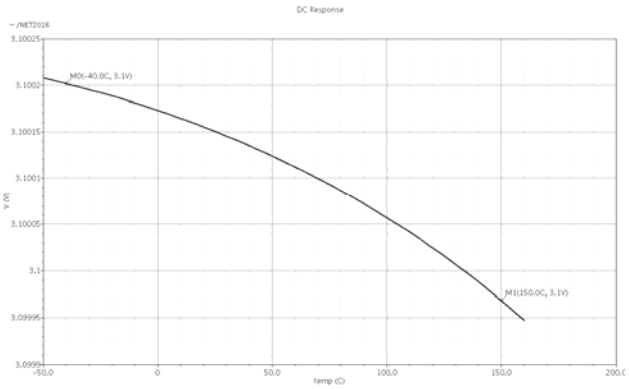

Fig. 11. Temperature drift of output voltage

IV. CONCLUSION

The paper presents the results from design and simulation of 0,35µm CMOS linear voltage regulator with high voltage power supply. The proposed circuits use an analog error amplifier, current source, start-up circuit, protection circuit, feedback and pass element. The input voltage is between 7V and 27V. The output voltage is 3,1V±0,2V.

Different simulations were carried out to verify the project. The simulations of error amplifier, output-to-input voltage ratio, line regulation, load regulation, PSRR and temperature drift of output voltage confirm emphatically the excellent performance of the designed circuit.

The results from the investigation will be used in the design of more complex application specific integrated circuits.

V. ACKNOWLEDGEMENT

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